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An overview of the deposition chemistry and the properties of *in situ* doped polysilicon prepared by low pressure chemical vapour deposition

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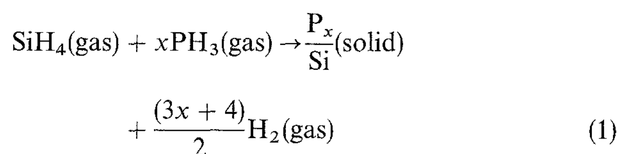
Low pressure chemical vapour deposition (LPCVD) has become the standard method for the fabrication of amorphous and polycrystalline silicon films in the semiconductor industry. However, as the trends towards lower temperatures, smaller dimensions and more complex geometries continue, it is becoming increasingly important to obtain a better fundamental understanding of the chemistry and properties of the layers deposited in order to achieve better control of the process. In this paper an overview is given of the chemistry, growth kinetics, electrical properties and structure of *in situ* doped polysilicon and of how these factors are related to reactor parameters. In addition, the effects of wafer cages on the within-wafer uniformity are discussed. Heat treatment using rapid thermal annealing has a significant impact on the electrical and structural properties of polysilicon and these effects are also examined.

1. Introduction

LPCVD has become the dominant process for the deposition of layers, such as polysilicon, silicon nitride and silicon dioxide, in the semiconductor industry, because it offers high film quality, large volume production, good process control and it is readily automated [1, 2].

Polycrystalline silicon is used for the gate electrode in metal–oxide semiconductor (MOS) devices, for the fabrication of high value resistors, for diffusion sources to form shallow junctions, for conduction lines and for ensuring ohmic contact between crystalline silicon substrates and overlying metallization structures [3]. For these and other applications it needs to be doped to lower its electrical resistance [3–5]. Three main methods are utilized for the introduction of dopants into silicon. These are ion implantation, diffusion and *in situ* doping during deposition. In the first two methods doping is carried out subsequent to deposition and normally requires a high temperature anneal in order to electrically activate the dopants [3]. *In situ* doping is attractive because doping and deposition can be achieved simultaneously in a single process at a low temperature [6], although to activate the dopants a high temperature anneal is still required. Therefore, the main advantage of *in situ* doping is that it saves one step in the manufacturing process. It is carried out in a standard LPCVD reactor [7] and involves the introduction of phosphine and silane into the furnace containing wafers. The overall reaction can be represented as follows



$$SiH_4(\text{gas}) + xPH_3(\text{gas}) \rightarrow \frac{P_x}{Si}(\text{solid}) + \frac{(3x+4)}{2}H_2(\text{gas}) \quad (1)$$

Very simply, silane decomposes on the wafer surface to yield solid silicon atoms and, simultaneously, phosphine cracks on the surface to give phosphorus atoms. This process results in the phosphorus atoms being incorporated into the growing silicon film. The properties of these films are highly dependent on the growth conditions and the process chemistry. An

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understanding of the effects of these factors enables the process engineer to develop recipes for reliable production processes and to solve process related problems.

Despite the attractive feature mentioned above of a single step process, if the *in situ* doped process is operated as a slightly modified standard LPCVD polysilicon process, a number of problems are encountered. These include very low growth rate, thickness non-uniformity and lack of control of film properties [6–9]. For example, the growth rate drops dramatically, from around $10\,\text{nm}\,\text{min}^{-1}$ in the undoped case, to about $0.5\,\text{nm}\,\text{min}^{-1}$ in the doped system. Then, there is considerable degradation in the thickness uniformity across the wafer, from better than $\pm 2\%$ to worse than $\pm 20\%$. Therefore, processing time is lengthened and the wafer area over which devices can be fabricated reproducibly and reliably is reduced. In this paper, results from studies of the process chemistry both in the gas phase, using mass spectrometry, and on the surface are reported and reviewed. Results on the effects of key reactor parameters on the growth rate, within-wafer uniformity, electrical properties and structure are also presented. In addition, the effects of annealing on the sheet resistance are related to the film structure. The insights into the process thus obtained are useful in helping to solve some of the problems mentioned and in developing an industrially viable process.

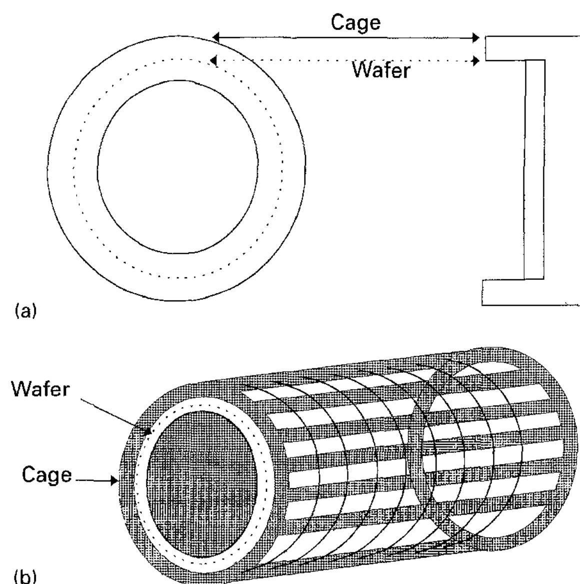


Figure 1 (a) Type 1 and (b) type 2 wafer cages used in the deposition of doped polysilicon films.

2. Experimental procedure

In this investigation, films were deposited onto sapphire $(1\bar{1}02)$ and oxidized silicon wafers of 5.1 and 7.6 cm diameter, by using a standard LPCVD system [7, 8]. Prior to deposition, wafers were cleaned in a 2:1 H_2SO_4/H_2O_2 mixture for 15 min followed by a 10 min rinse in running deionized water ($\simeq 18\,\text{M}\Omega$). The wafers were dried in a spin dryer with N_2 ambient.

Substrates were positioned vertically in a quartz boat at a spacing of 5 mm except for experiments where the effect of wafer spacing on growth rate was studied. Then wafer spacings in the range 5–25 mm were used. In selected experiments two types of wafer cages were employed, Fig. 1. Type 1 cage was simply a circular plate with a recess holding each wafer axially symmetric in the centre of the tube. Type 2 cage was made of quartz rods enclosing the wafers such as has been described before [7, 8]. The fused silica reactor tube was contained within a furnace with a temperature uniformity of $\pm 1\,^{\circ}\text{C}$ over the hot zone. As mentioned, silicon (with 0.1 μm of silicon dioxide) and sapphire substrates were used, the deposits on sapphire being employed for film thickness measurements after photolithography and etching of a suitable pattern. The deposition temperature was varied in the range 580–675 °C. The process pressure between 13 and 26 Pa was achieved by using a rotary pump and a throttle control valve. Accurate gas delivery was achieved using mass flow controllers for silane, disilane and phosphine. The gases used were 100% silane, 100% disilane and 1% phosphine in nitrogen, with electronic grade nitrogen as a purge gas. The silane and disilane flow rates were kept at $50\,\text{s}\,\text{cm}^3$, while the flow of the PH_3/N_2 mixture was varied to obtain different doping levels. Gas flow ratios of PH_3/SiH_4 and PH_3/Si_2H_6 (represented by γ) in the range $0\text{–}4 \times 10^{-3}$ were used. During loading and unloading of the reactor a positive pressure of nitrogen was used to ensure that oxygen and moisture contamination were kept to a minimum.

Annealing studies were performed using both conventional and rapid thermal methods under a variety of conditions. The conventional heat treatments were done at 900 °C or above in a quartz furnace. An AG Associates Heatpulse 2101 system was used for rapid thermal annealing. In both cases an atmosphere of dry nitrogen was used. Polysilicon samples in this study were not coated with oxide layers to prevent loss of dopant by evaporation. Sufficient protection was provided solely by the native oxide layer normally formed on a silicon surface at room temperature [10]. The film thicknesses were measured either using a Nanospec optical film thickness monitor, or after etching, with a Dektak surface profilometer.

Carrier concentration and spreading resistance were evaluated using an SSR spreading resistance two point probe. Dopant concentration depth profiles were evaluated by accurately bevelling the edge of the film to a known angle and taking spreading resistance readings at exact intervals along the bevel. A depth resolution of approximately 2% could be achieved in this way. Using this technique it was possible to quantify the trends in spreading resistance and carrier concentration within a sample and from one sample to another.

Sheet resistance was measured using a standard four point probe. The effects of various deposition parameters and annealing regimes on the sheet resistance were studied, giving an indication of the active carrier concentration to within $\pm 1\%$.

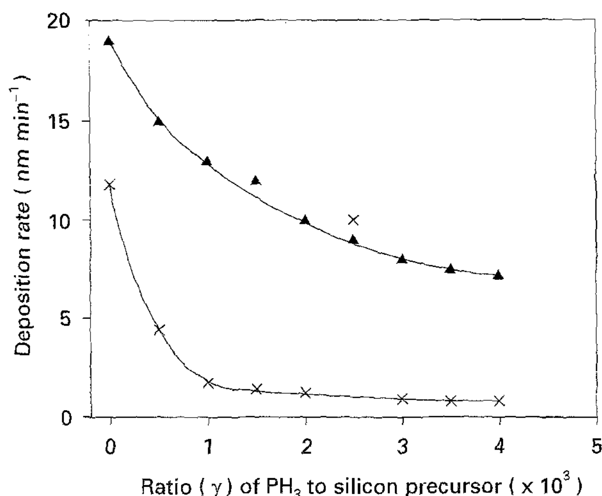
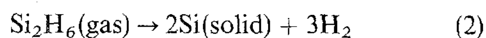


Figure 2 Deposition rate versus PH_3: silicon precursor ratio for (×) SiH_4 and (▲) Si_2H_6: deposition temperature, 630 °C; deposition pressure, 18.5 Pa; wafer spacing, 5 mm.

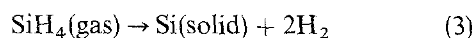
3. Results and discussion

3.1. Growth rate

The deposition rate of silicon as a function of the phosphine to silicon precursor ratio, both for silane and disilane is shown in Fig. 2. The films on the wafers were deposited at a temperature of 630 °C and a reactor pressure of 18.5 Pa. The deposition rate of undoped silicon from disilane was found to be approximately 19 nm min^{-1} compared to silane which yielded 11 nm min^{-1} in the same system under identical deposition conditions. It is interesting to note that the growth rate from disilane is just under twice that from silane. This is a little surprising at first sight since it has been shown [11] that disilane is much more strongly adsorbed on silicon than silane. For example, at 600 °C the sticking coefficient of SiH_4 is estimated to be $\simeq 5 \times 10^{-4}$, while that for Si_2H_6 is $\simeq 7 \times 10^{-2}$. This is reflected in the fact that to obtain a coverage of 0.01 monolayer requires an exposure of Si_2H_6 of about 400 times less than that for SiH_4. On the basis of a Langmuirian analysis of polysilicon growth [12] one would expect this to lead to a difference of about two orders of magnitude in growth rate. However, the strong adsorption of Si_2H_6 and its gaseous decomposition product SiH_2 could lead to a counteracting lower rate of surface mobility and decomposition of the adsorbate [13], although this would in itself be partially offset by Si_2H_6 giving two silicon atoms for each precursor molecule adsorbed compared with only one atom from an adsorbed SiH_4. The situation could be complicated even further by deposition from disilane, Equation 2, yielding 50% more H_2 than from silane decomposition, Equation 3, and adsorbed hydrogen acting as a growth inhibitor [14]



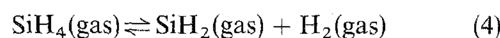
$$Si_2H_6(gas) \rightarrow 2Si(solid) + 3H_2 \quad (2)$$



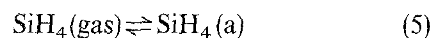
$$SiH_4(gas) \rightarrow Si(solid) + 2H_2 \quad (3)$$

For doped polysilicon, as the amount of PH_3 present in the reactor is increased the deposition rate drops significantly for both the SiH_4 and Si_2H_6. However, for disilane the deposition rate is down by a factor of only two, whereas for silane it is reduced by a factor of ten. Nakayama *et al.* [15], using a $PH_3/Si_2H_6/He$ system at a higher total system pressure (400 Pa) and temperature (665 °C) than reported here, obtained a much higher deposition rate, as might be expected, and they also found the deposition rate to be inhibited by PH_3. Using their data [15] if one plots the deposition rate against PH_3/Si_2H_6 ratio a trend similar to that shown in Fig. 2 is in fact observed, albeit with growth rates of about 20–25 times greater than the authors. Simon *et al.* [16] using an impinging jet type CVD reactor at a higher total system pressure (67 Pa) and a lower temperature (520 °C for hot wall and 550 °C for cold wall reactor) also observed that the deposition rate from disilane is inhibited by the addition of phosphine [16].

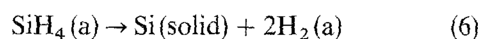
As has been discussed previously [17], the decrease in deposition rate with the addition of PH_3 cannot be simply due to a dilution effect, since keeping the deposition conditions the same and subsequently replacing the PH_3/N_2 mixture with pure N_2 does not produce any marked decrease in the deposition rate. It has therefore been postulated that PH_3 must be blocking the surface sites and inhibiting the deposition of silicon on the wafer surface [17, 18]. Meyerson and coworkers [18, 19] have demonstrated, using elegant surface science experiments, that PH_3 has close to a unit probability for adsorption, a, onto the silicon surface and is, thus, very effective in blocking surface sites for silane adsorption. A consideration [17] of the interaction of the various gaseous species with silicon surface has led to the relatively simple overall stoichiometric Equation 1 being represented by the following series of elementary steps



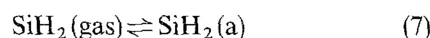
$$SiH_4(gas) \rightleftharpoons SiH_2(gas) + H_2(gas) \quad (4)$$



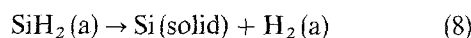
$$SiH_4(gas) \rightleftharpoons SiH_4(a) \quad (5)$$



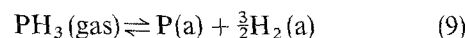
$$SiH_4(a) \rightarrow Si(solid) + 2H_2(a) \quad (6)$$



$$SiH_2(gas) \rightleftharpoons SiH_2(a) \quad (7)$$

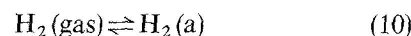


$$SiH_2(a) \rightarrow Si(solid) + H_2(a) \quad (8)$$



$$PH_3(gas) \rightleftharpoons P(a) + \tfrac{3}{2}H_2(a) \quad (9)$$

Hydrogen is also expected to be involved in an adsorption/desorption equilibrium



$$H_2(gas) \rightleftharpoons H_2(a) \quad (10)$$

In the case of disilane a similar series of elementary steps probably applies, but the deposition rate for doped polysilicon from a disilane and phosphine mixture can be, in some cases (see Fig. 2, with phosphine–silicon precursor ratio of 4×10^{-3}), about ten times higher than that obtained from silane and phosphine. This suggests that the PH_3 is not as effective in inhibiting deposition from disilane as it is for silane, and this is probably because Si_2H_6 is more strongly adsorbed than SiH_4 and there is more effective competition for surface sites by the silicon containing species; although one cannot discount the possibility that the process proceeds via different reaction mechanisms for the two cases.

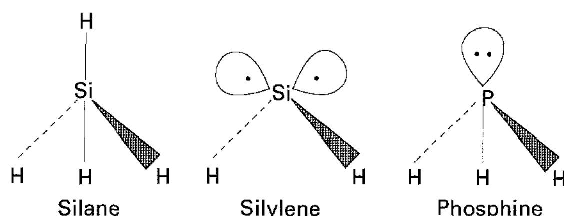


Figure 3 Structures of various species involved in the deposition process.

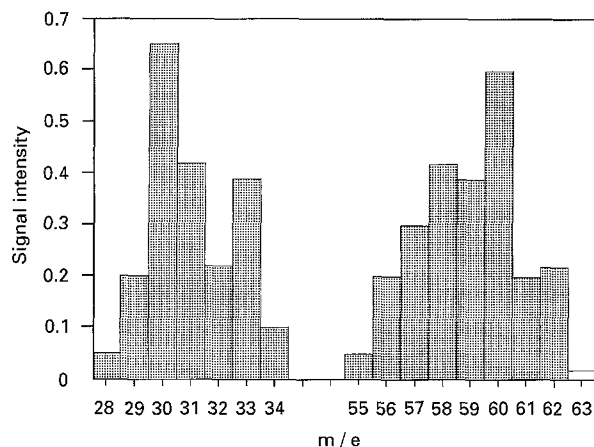


Figure 4 Mass spectra for disilane at room temperature (25 °C) without any deposition in the reactor.

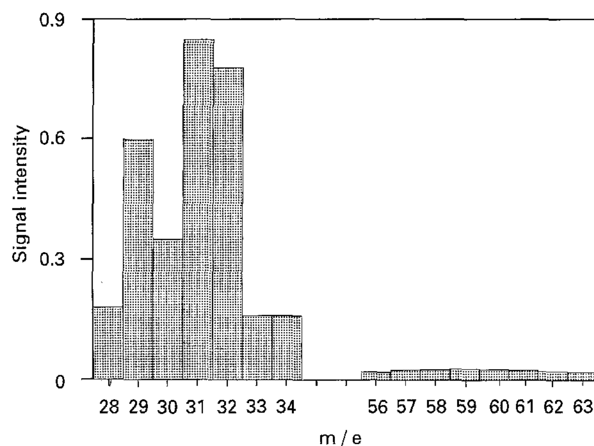
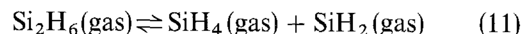


Figure 5 Mass spectra for disilane during deposition in the reactor at 630 °C.

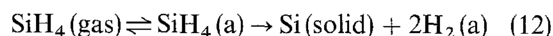
Now consider the mechanistic possibilities a little further. As shown in Fig. 3, phosphine has a lone pair of electrons and is expected to adsorb strongly onto a silicon surface with dangling bonds [13]. The ready adsorption of a phosphorus species onto the surface will inhibit the adsorption of silane, Equation 5, which is a saturated molecule and which therefore does not adsorb as strongly. This thus results in a marked decrease in the deposition rate. As has been mentioned, disilane adsorbs much more strongly than silane and so could compete effectively with PH_3 for surface sites, but there is another possible route by which Si_2H_6 could compete for adsorption sites.

Examination of mass spectrometer data reveals gas phase decomposition of disilane as shown in Figs 4 and 5. Mass spectral analysis at near room temperature shows (Fig. 4) two sets of peaks, one associated with silane (m/e 28–32) and the other set with disilane (m/e 56–62), with the intensities of both sets of peaks being of a similar magnitude. When the reactor temperature was raised to about 630 °C, the intensity of the peaks associated with disilane decreased, not unexpectedly because of silicon deposition occurring. However, in addition those associated with silane generally increased (Fig. 5) and the integrated area for the low m/e set is about twice that found at room temperature. This suggests that disilane fragments readily at the deposition temperature as shown in Equation 11

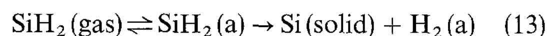


$$Si_2H_6(\text{gas}) \rightleftharpoons SiH_4(\text{gas}) + SiH_2(\text{gas}) \qquad (11)$$

Thermodynamics favours the formation of SiH_2 and SiH_4 rather than two SiH_3 species from the decomposition of Si_2H_6 [20, 21]. The SiH_4 and SiH_2 species can then both decompose to yield silicon atoms on the surface



$$SiH_4(\text{gas}) \rightleftharpoons SiH_4(\text{a}) \rightarrow Si(\text{solid}) + 2H_2(\text{a}) \qquad (12)$$



$$SiH_2(\text{gas}) \rightleftharpoons SiH_2(\text{a}) \rightarrow Si(\text{solid}) + H_2(\text{a}) \qquad (13)$$

Hydrogen can also adsorb/desorb as before in Equation 10. The important difference from the case where SiH_4 alone is decomposing is that the silylene (SiH_2), is a highly reactive unsaturated species with two unpaired electrons (Fig. 3) and therefore it can compete very effectively for surface sites with phosphine. Thus, the blocking effect of phosphine would be dramatically less pronounced if SiH_2 were the prime species involved in the growth of polysilicon.

This is clearly an alternative explanation to strong disilane adsorption for the weaker effect on growth rate of PH_3. Whichever mechanism may actually hold, an overall picture of the deposition of undoped and *in situ* doped silicon from silane and disilane can be represented pictorially as shown in Fig. 6. Fig. 6a shows the reaction scheme which was postulated earlier for the deposition of silicon from silane alone [17], where a very small amount of disilane is formed as a gaseous product. For deposition from disilane Fig. 6(b), the phosphine inhibits the growth rate of silicon from Equation 12 in exactly the same way as it does in the case for silane, but SiH_2 decomposition on the surface, Equation 13, will be largely unaffected due to its highly reactive nature, as already discussed.

3.2. Uniformity

Fig. 7 shows the variation with radial distance of the deposition rate on a wafer and the improvement in the uniformity resulting from the use of wafer cages for polysilicon deposition from Si_2H_6 in the presence of PH_3. Without the use of a wafer cage the within-wafer uniformity is good to a distance from the centre of the wafer of about 10 mm and then degrades rapidly with a growth rate $> 70\%$ higher near the edge of the wafer than at the centre. However, if a wafer cage is employed good uniformity is observed up to a radial distance of 18 mm and a variation in the uniformity of about only 20% greater than that at the centre near the wafer edge results, which is a significant improvement over the wafer without the cage. A similar behaviour is also observed when silane is used as a silicon precursor [8].

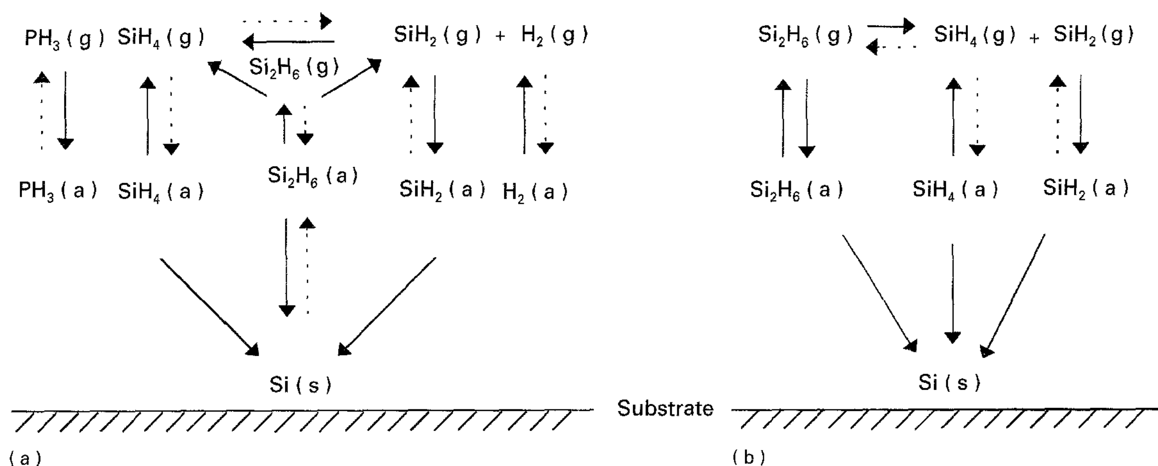


Figure 6 A pictorial representation of deposition of undoped and *in situ* doped silicon from (a) silane and (b) disilane.

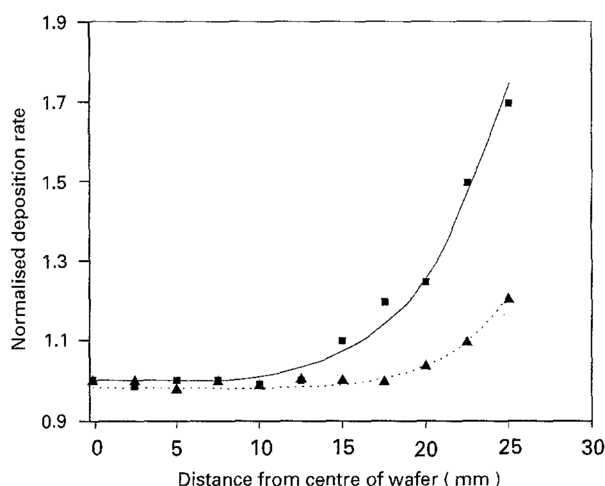


Figure 7 Normalized deposition rate from PH_3/Si_2H_6 versus radial distance across a wafer: (■) without cage, and (▲) with cage.

Considerations of kinetics and transport for silicon deposition from monosilane show that the radial variation of growth cannot be due to the depletion of SiH_4 in the inter-wafer spacing [17]. The rate of mass transport is much greater than the rate of surface reaction. However, in the presence of PH_3 when deposition from SiH_4 species is blocked, the primary route is via SiH_2 (cf. Fig. 6), and this species can readily deplete as it travels from the edge of the wafer to the centre [17]. The mass transfer coefficient for SiH_2 is expected to be very similar to that for SiH_4 since the diffusion coefficient is similar and the diffusion lengths are just the same. The rate constant for deposition of silicon from SiH_2 is, though, about 10^4 times that for growth from SiH_4 [22]. Therefore, since the rate of surface reaction is much greater than the rate of diffusion the growth rate from SiH_2 will be transport controlled rather than kinetically controlled. The wafer cages shown schematically in Fig. 1, can effectively trap very reactive species, such as SiH_2, in the annular region before they enter the wafer region and reduce the concentration gradient between the annular region and the centre of the wafer. Thus, the within-wafer uniformity is dramatically improved. A similar argument can be invoked for the case of deposition from disilane in the presence of phosphine.

For deposition from disilane the situation is further complicated, as already discussed, by the possibility of deposition from the very reactive Si_2H_6 species itself, and so this can deplete just like SiH_2 as it travels from the edges of the wafers to the centres resulting in a strong contribution to the non-uniformity. Since disilane has a mass which is nearly twice that of silane the rate at which it diffuses between wafers is likely to be slower than species containing single silicon atoms (SiH_2 and SiH_4) and this should make the depletion situation slightly worse; this is indeed found if one compares data plotted as in Fig. 7 for disilane with silane. As mentioned above, the use of wafer cages results in a significant improvement in the uniformity of the deposits and as discussed before the cages are effective in trapping highly reactive species such as disilane.

For practical purposes the type 2 wafer cage shown in Fig. 1 needs to be customized for each change in the deposition parameters, because altering the deposition conditions can effect the process chemistry both in the gas phase and on the surface and one needs to match the cage area [8] and positioning to account for any changes in the concentrations of the various species involved in the deposition process. The type 1 cage is much simpler in construction and therefore is more attractive for production purposes. Alterations to this cage involve simple changes in the diameter of the plate. Both types yield significant improvements to within-wafer uniformity. Other solutions to improve within-wafer uniformity have been suggested and involve reducing the wafer edge to reactor wall distance [23] and using reduced reactor pressure [9].

Fig. 8 shows the effect of wafer spacing on the growth rate and resistivity for the deposition of silicon from silane. As the wafer spacing is increased the growth rate also increases with a corresponding decrease in resistivity. In addition, there is a dramatic improvement in within-wafer uniformity with increasing wafer spacing as shown in Fig. 9. This is consistent with results published previously for the deposition of semi-insulating polysilicon (SIPOS) and for *in situ* doped polysilicon [10, 17, 23]. This gives additional support for the idea that the process has imposed transport limitations [17]. If there were no transport

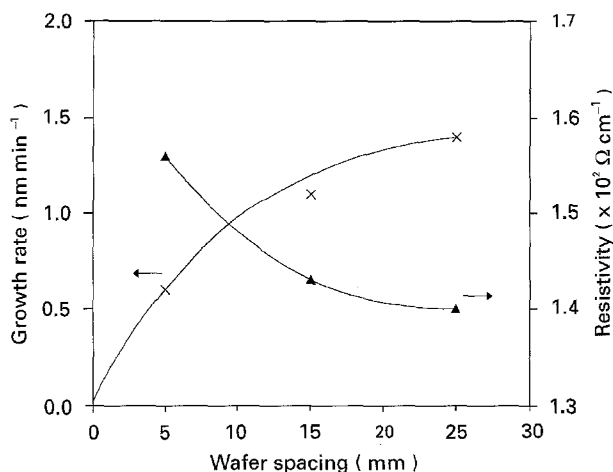


Figure 8 The effect of wafer spacing on the growth rate (×) and resistivity (▲) for silane: deposition temperature, 650 °C; deposition pressure, 19.8 Pa; γ, 4×10^{-3}.

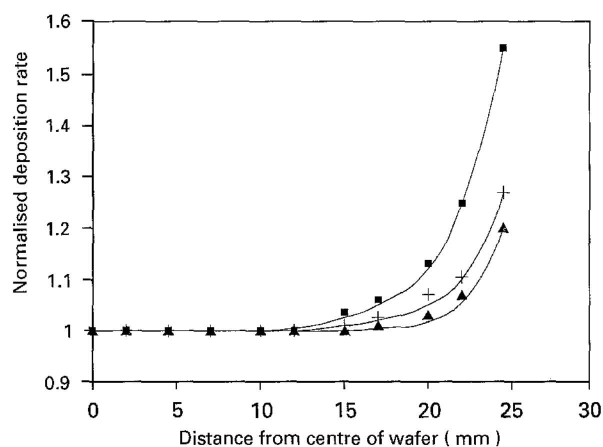


Figure 9 Variation of normalized growth rate with distance from the centre of the wafer at different wafer spacings of (■) 5 mm, (+) 15 mm and (▲) 25 mm: deposition temperature, 650 °C; deposition pressure, 19.8 Pa; γ, 4×10^{-3}.

limitations, the growth rate and the uniformity would be unaffected by the change in wafer spacing.

Further evidence for the involvement of transport control in the deposition process is given by the temperature dependence of growth rate. Fig. 10 shows the effect of temperature on the deposition rate from silane in the presence of PH_3. The logarithm of the growth rate at the centre of the wafer is plotted against the reciprocal of the temperature in an Arrhenius type plot to allow calculation of the activation energy, E_a. The values of E_a obtained from Fig. 10 and from the results of other workers are given in Table I. There is a large variation in the activation energies. It is difficult to obtain a meaningful comparison of activation energy because of large variations in the deposition conditions which have a significant influence on the deposition chemistry and the relative roles of kinetics and mass transport. The activation energy values obtained will have both a mass transport contribution and a kinetic contribution. Mass transport limited processes are generally less sensitive to temperature and are characterized by lower activation energies compared with reaction limited processes. Experimental work carried out which moves between these extremes of deposition will be characterized by an

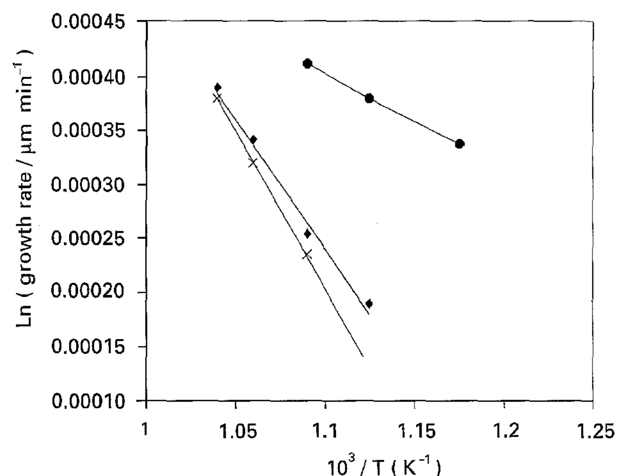


Figure 10 The effect of temperature, *I*, on the deposition rate: deposition pressure, 19.8 Pa; γ, 4×10^{-3} (×), 2×10^{-3} (◆), 2×10^{-4} (●).

TABLE I Activation energies for silane and disilane both doped and undoped

	γ	E_a (kJ mol^{-1})	Reference
SiH_4	0.000	67	
PH_3/SiH_4	0.001	75	[24]
PH_3/SiH_4	0.010	96	
PH_3/SiH_4	2.00×10^{-4}	82	
PH_3/SiH_4	2.00×10^{-3}	196	Present work
PH_3/SiH_4	4.00×10^{-3}	230	
SiH_4	0.00	67	
B_2H_6/SiH_4	0.10	46	[22]
B_2H_6/SiH_4	5.00	29	
AsH_3/SiH_4	0.01–0.05	147	
SiH_4	0	160	[25]
Si_2H_6	0	139	
Si_2H_6	0	244	
PH_3/Si_2H_6	6.67×10^{-5}	256	[15]
PH_3/Si_2H_6	1.67×10^{-3}	293	
PH_3/Si_2H_6	4.00×10^{-2}	348	

intermediate value for E_a. For example, from the table it can be seen that Kurokawa [24] found activation energies of 67, 75 and 96 kJ mol^{-1} for $\gamma = 0, 0.001$ and 0.01, respectively, at a pressure of 52 Pa using He as a carrier gas, compared to 82, 196 and 230 kJ mol^{-1} for the same values of γ in the current work but carried out at a lower total pressure of 18.5 Pa and using N_2 as a carrier gas. This pressure dependence trend agrees with that obtained by Farrow [22] supporting the mass transport hypothesis. As the reactor pressure is increased there is an increase in the mass transport contribution to growth and hence a lowering of activation energy. For doped silicon deposition from silane, the activation energy values increase as the amount of phosphine added to silane increases in agreement with other workers [24]. An increase in activation energy with the addition of dopant has also been observed for arsine which is also an *n*-type dopant [22]. As mentioned earlier *n*-type dopants are effective inhibitors of deposition of silicon due to their blocking of surface sites, hence the kinetic activation required for deposition will be higher. For deposition

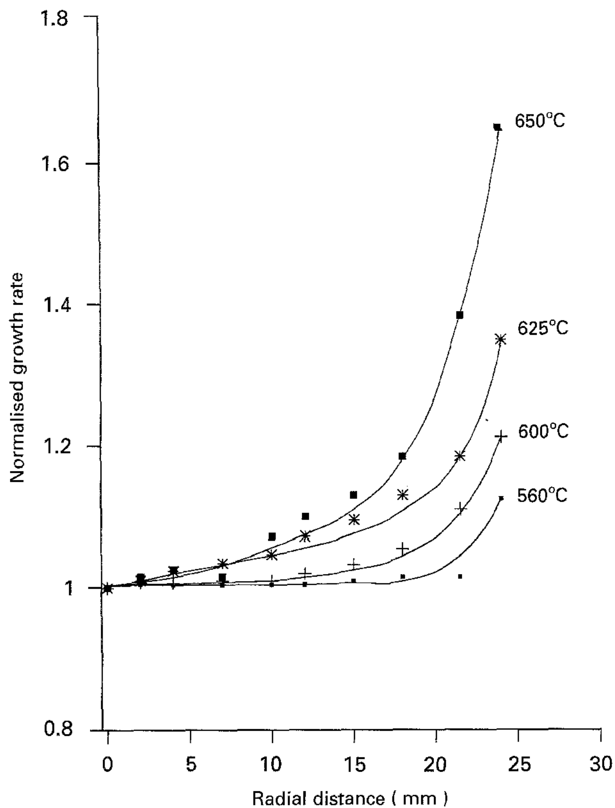


Figure 11 The effect of temperature on the within-wafer uniformity: at (■) 650°, (★) 625 °C, (+) 600 °C and (■) 560 °C; deposition pressure, 19.8 Pa; γ, 4×10^{-3}.

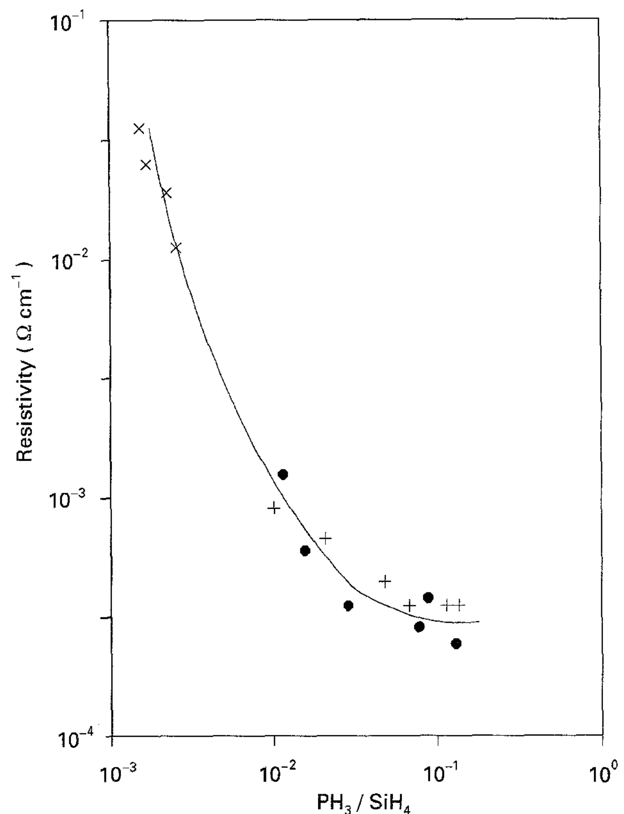


Figure 12 Resistivity as a function of phosphine to silane ratio [4]. Key: (x) [4]; ● [24] at 630 °C; (+) [24] at 650 °C and annealed in N_2 at 1800 °C.

from disilane in the presence of phosphine the activation energy trend from the data of Nakayama *et al.* [15] is similar to that obtained for silane, again as would be expected for inhibition by PH_3. In the absence of phosphine, the activation energy for deposition of silicon from disilane would be expected to be lower than that from pure silane since disilane is a more reactive species. This seems to be the case when depositions are done under identical conditions [25].

Still further evidence for the hypothesis that transport control affects the deposition comes from examining the effects of temperature on the within-wafer uniformity, as shown in Fig. 11. As the temperature is increased from 560 to 650 °C there is a dramatic degradation in the within-wafer uniformity. The increase in temperature, T, will result in rapid increase in the rate of surface reaction (R) with the rate being directly proportional to $\exp^{(-E_a/RT)}$. At the same time the rate of diffusion between the wafers also increases but at a much slower rate, the diffusion rate being approximately proportional to $T^{3/2}$. Thus, the difference in the rate of reaction and the rate of diffusion is much greater at higher temperatures resulting in more severe depletion of reactants in the inter-wafer spacing and hence a degrading in the uniformity, i.e. a mass transport regime becomes more dominant at higher temperatures.

3.3. Electrical properties

Fig. 12 demonstrates the changes in resistivity as a function of phosphine to silane ratio. For ratios up to 10^{-2} there is a rapid decrease in the film resistivity, after which the resistivity decrease begins to slow down and eventually levels off probably corresponding to the maximum solid solubility of phosphorus in silicon. For γ in the range 10^{-3}–10^{-1}, the observed trend in film resistivity is very similar to that reported previously by other workers [24, 26]. However, Taniguchi *et al.* [26] carried out experiments over a much wider range of γ and concluded that below 3×10^{-5} the dopant atoms incorporated compensate for the native defects present mainly in the grain boundary region until the native defect density is reached. The resistivity thus decreases more slowly with increasing PH_3/SiH_4 for $\gamma = 3 \times 10^{-5}$ to $\gamma \approx 10^{-3}$ and then decreases more rapidly, as is shown by the data in Fig. 12.

Fig. 13 shows the change in resistivity across a wafer for $\gamma = 4 \times 10^{-3}$. Near the centre of the wafer the resistivity is approximately constant, while there is a reduction in the value of resistivity towards the edge of the wafer. This trend mirrors that of the thickness variation across the wafer, suggesting a correlation between thickness and resistivity. Further evidence of this relationship is shown in Fig. 8, where the wafer spacing has been varied while all other parameters, such as pressure, temperature and gas flow ratios, were kept constant. As we have seen, an increase in wafer spacing results in an increase in film thickness; a 5 mm spacing gave films of 0.2 μm thickness, whereas a spacing of 25 mm produced films of 0.38 μm thickness. A decrease in resistivity with increased wafer spacing is also evident (Fig. 8). The work of Lu *et al.* [27], who studied the doping of polysilicon by

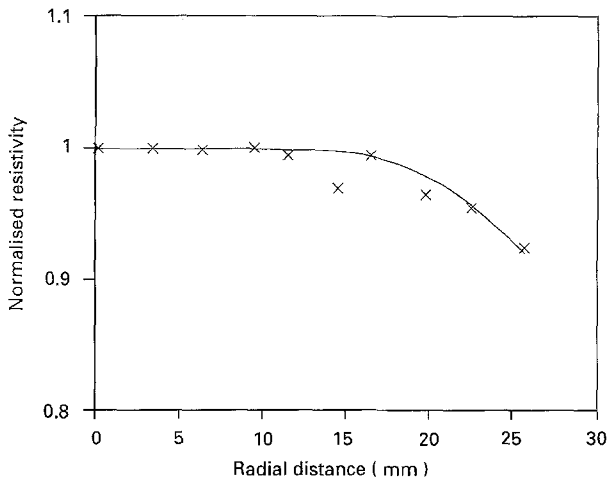


Figure 13 Normalized resistivity across a wafer as a function of radial distance: deposition temperature, 650 °C; deposition pressure, 19.8 Pa; γ, 4×10^{-3}.

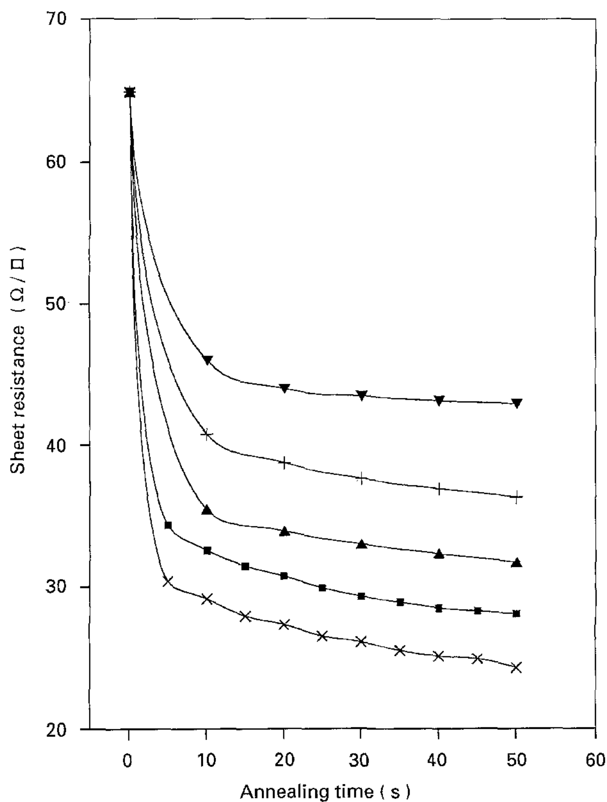


Figure 14 Resistivity versus rapid thermal annealing time at temperatures of 950 °C (▼), 1000 °C (+), 1050 °C (▲), 1100 °C (■), and 1150 °C (×).

ion implantation further supports this observation by demonstrating that the resistivity increases with decreasing film thickness due to carrier trapping in grain boundaries (see below). Mandurah *et al.* [28] also reported a decrease in resistivity with increasing thickness on diffused dopants. Hall measurements revealed a higher mobility at the surface of thick films.

The effect of annealing time on the sheet resistivity for several different temperatures using dry nitrogen is reported in Fig. 14. Initially there is a sharp drop in the resistivity as the dopant atoms are activated. After further annealing the reduction in resistivity is less prominent. This behaviour was observed for all temperatures. As the annealing temperature is raised, although the trends are similar, lower sheet resistance values are obtained.

Several mechanisms have been proposed to explain the variation in resistivity with film thickness in polysilicon thin films [27]. The decrease in resistivity with increasing thickness may be the result of two different scattering mechanisms. The first involves the scattering of carriers at the polysilicon–oxide interface. As carriers are scattered their mobility is reduced. The number of collisions with the interface, i.e. the probability of collision, being greater in thin films than thick films, and so the resistivity will decrease with increasing film thickness. This mechanism is an unlikely one for *in situ* doped polysilicon, because if an oxide layer were deliberately formed on the surface straight after deposition one would expect the resistivity to increase. However, practical results [29] reveal that the addition of an oxide capping layer has no significant effect on the resistivity. The second mechanism involves the scattering of carriers at horizontal grain boundaries. With thinner films the proportion of carriers likely to be scattered at these boundaries is greater, resulting in higher resistivities. Transmission electron microscope (TEM) micrographs of the LPCVD polysilicon films show a structure which has a predominance of vertical grain boundaries [7, 29], with horizontal boundaries being rare. The films had a "V"-shaped cross-sectional structure [7, 30] and it is therefore also unlikely that this mechanism plays the major role in reducing the resistivity with increasing thickness [31].

Another explanation for higher resistivity values with decreasing thickness is that they could be attributed to dopant loss from the surface of thinner films. The surface area to volume ratio is larger than for thicker films and therefore the loss of dopant from the thinner films could have a greater impact on the resistivity. However, there are two arguments which challenge this statement. Firstly, the loss of dopant from the surface is expected to be greater at higher deposition or annealing temperatures as the dopant diffusion rate increases with increased temperature. Secondly, it is expected that if the film is capped with an oxide layer then there will be an accumulation of dopant near the surface. A silicon oxide cap was deposited by chemical vapour deposition onto the film at 400 °C, and carrier concentration and spreading resistance measurements were taken [29] for both capped and uncapped material. This revealed that there was no significant loss of dopant from the surface, the profiles being virtually identical. This experiment was carried out on a wafer divided into two halves with the aid of photolithography and therefore the deposition and annealing conditions were identical.

The most likely explanation for the measured reduction in resistivity of the thicker films involves a consideration of the polysilicon film structure [31]. Polycrystalline material may be viewed as being made up of two distinct regions, the crystallites and the grain boundaries. The crystallites are composed of ordered atoms, whereas the grain boundaries are composed of disordered atoms which represent the

transition region between crystallites. The carrier-trapping models consider that the grain boundaries contain trapping centres for the dopant atoms which allow two effects to be proposed. The first involves the reduction in the number of free carriers, while the second involves the formation of a potential barrier which impedes the motion of the free carriers. Both of these effects could be responsible for the increase in resistivity in thinner films. In the thicker films the resistivity is reduced due to the reduction in the number of grain boundaries. The radial variation of the resistivity noted could be due to the variation in film thicknesses, but could also be attributed to variations in dopant concentration.

Trainor [32] studied the effect of wafer radial distance on both the total phosphorus content and resistivity. He observed a total phosphorus increase by a factor of five; while the resistivity, representing active phosphorus, decreased only by about 30%. It has been shown above that there is a higher growth rate at the edge of the wafer compared with the centre. This higher growth rate could lead to less crystalline growth resulting in smaller grains. Hence at the edge of a wafer one would expect more grain boundaries and a resulting greater loss of active dopant by segregation; TEM micrographs do in fact show smaller grains at the wafer edge [32]. Thus, this model would predict a higher resistivity at the edge compared with the centre. In addition, since it has been shown that at the edge of a wafer growth occurs mainly from SiH_2 species which can effectively compete for surface sites with PH_3, one might expect less total phosphorus at a wafer edge than in the centre. Therefore, based on the considerations discussed so far, the opposite effects to those observed would be expected, and one has to look for an additional explanation. This explanation must allow a greater growth from SiH_2 and at the same time a greater total incorporation of phosphorus. Workers in the field of gas phase kinetics [33] have demonstrated the rapid conversion of PH_3 to monosilylphosphine in the presence of SiH_4 pyrolysis. If one extends the deposition model described earlier to allow growth not just from SiH_2 but from SiH_2PH_2 as well, this could explain both the radial variation of growth rate and total phosphorus content. The smaller variations in resistivity with radial distance could then be attributable to the increase in the number of grain boundaries expected at the wafer edge and a corresponding higher percentage of inactive phosphorus in these grain boundaries [7].

A wafer cage has been seen to give uniform growth and this has been attributed to the evening out of the concentration profile of reactive species in the spacing between wafers. With the extended model [7] this would be expected to even out also the total phosphorus content. In addition, since the growth rate is now the same over the whole wafer, the degree of crystallinity and hence the electrical properties of the layer would be expected to be uniform. Further studies need to be made to verify this qualitative analysis and to put it on a more quantitative basis.

When the *in situ* doped films were annealed at 950 °C under dry nitrogen (see Fig. 14) it was noted that the resistance decreased sharply and then levelled off. This behaviour can also be explained in terms of carrier-trapping and grain growth. Upon annealing the carriers which reside within the grain boundaries (initially immobile) are given enough energy for them to become mobile and thus enter crystallites where they become active and thus cause the resistivity to fall. This is probably associated with the initial rapid decrease in sheet resistance. A more prolonged anneal causes the initial activation of dopant atoms to be followed by grain growth, which reduces the resistance even further; but this effect is smaller than the activation of dopants. It is probably linked to the scattering mechanisms described above.

4. Conclusions

Problems inherent in the growth of *in situ* doped polysilicon and the work undertaken to understand and find solutions for them has been reviewed. The deposition behaviour for doped silicon, the origin of non-uniformity and low growth rate have been discussed. Practical solutions to these problems have been presented involving the use of the more reactive silicon precursor disilane and two types of wafer cages. It has been shown that a within-wafer non-uniform thickness leads to non-uniformity of the electrical characteristics. Several basic physical mechanisms have been suggested and examined to explain this phenomenon, and it has been concluded that these variations are a function of the film thickness, active phosphorus content and structure. It is postulated that changes in the film structure lead to changes in the active to total dopant rates (P_A/P_T) which is directly related to the observed electrical properties.

References

1. M. L. HITCHMAN and K. F. JENSEN, in "Chemical vapour deposition: principles and applications", edited by M. L. Hitchman and K. F. Jensen (Academic Press, London. 1993) Ch. 1.
2. P. JOHN, in "The chemistry of the semiconductor industry", edited by S. J. Moss and A. Ledwith (Blackie, Glasgow, 1987) Ch. 5.
3. S. WOLF and R. N. TAUBER, "Silicon processing for VLSI era, process technology", Vol. 1 (Lattice Press, Ca, 1986) Ch. 6.
4. M. L. HITCHMAN and W. AHMED, *Vacuum* **34** (1984) 979.
5. M. L. HITCHMAN, C. W. JONES, J. ZHAO and S. SHAMLIAN, *Advan. Mater. Optics & Elec.* **2** (1993) 123.
6. W. AHMED and D. B. MEAKIN, *J. Crys. Growth* **79** (1986) 394.
7. M. L. HITCHMAN and K. F. JENSEN, in "Chemical vapour deposition: principles and applications", edited by M. L. Hitchman and K. F. Jensen (Academic Press, London, 1993) Ch. 4.
8. K. F. JENSEN, M. L. HITCHMAN and W. AHMED, in "Proceedings of the Fifth European CVD, Upsala Sweden, 1985, edited by J. O. Carlsson and J. Lindstrom (Univ. of Upsala) p. 144.
9. W. AHMED, R. D. PILKINGTON and D. B. MEAKIN, *Thin Solid Films* **202** (1991) 97.
10. W. AHMED, PhD thesis, University of Salford, Salford (1986)
11. S. M. GATES, D. B. BEACH, R. INBIHL, B. A. SCOTT and J. E. DENMUTH, *J. Vac. Sci. Technol.* **5** (1987) 628.
12. M. L. HITCHMAN, J. KANE and A. E. WIDMER, *Thin Solid Films* **59** (1979) 231.

13. M. L. HITCHMAN, and J. F. ZHAO, *J. de Phys. IV, Colloque C3* **3** (1993) C-115.
14. K. F. ROENIGK and K. F. JENSEN, *J. Electrochem. Soc.* **132** (1985) 448.
15. S. NAKAYAMA, H. YONEZAWA and J. MUROTA, *Jpn. J. Appl. Phys.* **23(7)** (1984) L493.
16. J. SIMON, R. FEURER, A. REYNES and R. MORANCHO, *J. de Phys. IV, Colloque C3* **3** (1993) 99.
17. M. L. HITCHMAN, W. AHMED, S. SHAMLIAN and M. TRAINOR, *Chemtronics* **2** (1987) 147.
18. B. S. MEYERSON and W. OLBRICHT, *J. Electrochem. Soc.* **131** (1984) 2361.
19. B. S. MEYERSON and M. L. YU, *ibid.* **131** (1984) 2366.
20. M. GUEYE, E. SCHEID, P. TAURINES, P. DUVERNEUIL, D. BRELLE-DASPET and J. P. COUDERC, *J. de Phys. IV, Colloque C2, suppl. au J. de Phys. II* **1** (1991) C2-63.
21. P. HO, M. E. COLTRIN, J. S. BINKLEY and C. F. MELIUS, *J. Phys. Chem.* **89** (1985) 4647.
22. R. F. C. FARROW, *J. Electrochem. Soc.* **121** (1974) 899.
23. M. L. HITCHMAN and J. KANE, *J. Crys. Growth* **55** (1981) 485.
24. H. KUROKAWA, *J. Electrochem. Soc.* **129** (1982) 2620.
25. K. NAKAZAWA, *J. Appl. Phys.* **69** (1991) 1703.
26. M. TANIGUCHI, M. HIROSE, Y. OSAKA, S. HASEGAWA and T. SHIMIZU, *Jpn. J. Appl. Phys.* **19** (1980) 665.
27. N. C. LU, C. Y. LU, M. K. LEE, C. C. SHIH, C. S. WANG, W. REUTER and T. T. SHENG, *J. Electrochem. Soc.* **131** (1984) 897.
28. M. M. MANDURAH, K. C. SARASWAT and T. I. KAMINS, *ibid.* **126** (1979) 1019.
29. W. AHMED and R. D. PILKINGTON, *J. Electronic Mater* (1995), submitted.
30. W. AHMED and E. AHMED, *Mater. Chem. Phys.* **37** (1994) 289.
31. J. W. SETO, *J. Electrochem. Soc.* **46** (1975) 5247.
32. M. TRAINOR PhD thesis, University of Strathclyde, Glasgow (1989).
33. J. BLAZEJOWSKI and F. W. LAMPE, *J. Photochem.* **20** (1982) 9.

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